

Experimental demonstration of the effect of field damping layers in quantum-dot intermediate band solar cells

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ABSTRACT

Intermediate band solar cells must demonstrate the principle of voltage preservation in order to achieve high conversion efficiencies. Tunnel escape of carriers has proved deleterious for this purpose in quantum dot intermediate band solar cells. In previous works, thick spacers between quantum dot layers were demonstrated as a means of reducing tunnel escape, but this approach is unrealistic if a large number of quantum dot layers have to be grown. In this work we report experimental proof that the use of field damping layers is equally effective at reducing tunnel carrier escape, by reducing the potential drop in the QD-stack and the associated electric field. Moreover, we demonstrate that the fact that tunnel carrier escape takes place under short-circuit conditions does not imply that voltage preservation cannot be achieved. We describe a theory that relates the evolution of the tunnel escape to bias voltage and the preservation of the voltage in an IBSC. Temperature and voltage-dependent quantum efficiency measurements, temperature dependent open-circuit voltage measurements and calculations of the internal electric field in IBSCs serve as the basis of the proposed theory.

1. Introduction

Intermediate band solar cells (IBSCs) [1] must fulfill the *voltage preservation* principle in order to achieve high conversion efficiencies. This principle states that the output voltage of such a solar cell is only fundamentally limited by the bandgap, E_G , of the intermediate band (IB) host material. The two additional sub-bandgaps resulting from the presence of the IB – E_{H1} for the larger and E_L for the smaller – contribute to an increase of the photocurrent of the solar cell but do not set a limit to the operation voltage. Three quasi-Fermi levels (QFLs) are needed to describe the electronic population of the three bands of an IBSC working in accordance to the voltage preservation principle: ε_{Fe} , ε_{FIB} and ε_{Fh} , for the conduction band (CB), IB and valence band (VB), respectively [2]. The voltage preservation principle has been verified so far in IBSC prototypes using InAs/GaAs quantum dots (QD) [3,4] or Ti-doped GaAs [5] as the IB material. The demonstration consists in measuring a photo-voltage larger than E_{H1}/e and, in the limit, close to E_G/e , where e is the electronic charge. In all cases this has only been possible at low temperatures, because of the existence of a fast thermal escape of carriers from the IB to the CB at room temperature (RT) [6], which prevents the QFL split between these two bands.

For QD-IBSC prototypes, it has been demonstrated that tunnel-assisted carrier escape between the IB and the CB must also be eliminated for achieving voltage preservation [3,6]. Tunnel carrier escape is activated by the electric field that exists in the QD-stack, generally placed between p-doped and n-doped emitters. Electron tunneling between the IB and the CB can be avoided by growing thick spacers between two consecutive QD-layers [6]. This approach is not, however, without disadvantage. Thick spacers set a practical limit to the number of QD-layers that can be grown, by increasing both the time and the cost of each sample growth. A large number of QD-layers is desired to enhance sub-bandgap absorption, which is weak in current QD-IBSC prototypes [7]. The challenge remains in being able to fabricate IBSCs containing a large number of QD-layers and, at the same time, avoiding carrier tunnel escape. In Ref. [8] the use of field damping layers (FDLs) was proposed to sustain a large part of the potential drop between the emitters, so that the QD-stack is placed in a flat-band zone of the device. This approach aims to avoid tunneling between the IB and the CB (this will be discussed in detail later) without the need for increasing the thickness of the spacers between QD-layers, but no empirical evidence in this regard has yet been reported.

In this work we investigate experimentally the voltage preservation principle in three different QD-IBSC prototypes. For this, we analyze the temperature and voltage dependence of their quantum efficiency (QE), evaluating the impact of the spacer thickness and the

FDLs. Finally we discuss how sub-bandgap QE, tunnel escape and voltage preservation are related.

2. Material and methods

2.1. Sample description

Three batches of samples, SC1, SC2 and SC3, were manufactured. SC1 coincides with S3 in Ref. [3] and with SB in Ref. [6]; the structure of SC2 is described in Ref. [8] and coincides with SC in Ref. [6] and S2 in Ref. [3]; and SC3 coincides with S1 in Ref. [3]. Detailed structures and growth conditions for these samples can be found in Refs. [3,6,8]. We indicate here the most relevant characteristic of these samples for the present work.

All samples contain a stack of InAs/GaAs QDs. Samples SC1 and SC3 correspond to a basic QD-IBSC layer structure: p-emitter/QD-stack/n-emitter. SC1 contains 30 layers of QDs, while SC3 contains only 10 layers. SC1 has thick (84 nm) spacers while SC3 has thin (10 nm) spacers. SC2 contains 10 layers of QDs separated by thin (13 nm) spacers. The key difference with respect to the other two samples is that the structure of SC2 includes two extra layers: a 100 nm thick layer of undoped GaAs between the n-doped emitter and the QD-stack, and a 170 nm thick layer of lightly doped n-GaAs between the QD-stack and the p-doped emitter. These layers perform as FDLs, sustaining most of the junction built-in potential, V_{bi} , so that QDs can be driven to a flat-band potential region under forward bias. These details, along with other, some of which will be introduced later, are summarized in Table 1. The simplified band diagrams under short-circuit conditions for each sample (SC1, SC2 and SC3, from left to right) are sketched in Fig. 1a. These sketches are intuitive graphical illustrations of the impact of both the spacer thickness and the FDLs in the band diagram of a QD-IBSC. They will serve also to define some parameters used in the discussion of our results. To preserve a common vertical scale, the band diagram of SC1, which is much thicker than the other two samples, is broken at some points. In Section 4 we will present calculation results of the actual band diagram in the QD regions of our samples.

2.2. Measurement conditions

Samples were mounted on a copper disk and placed in a closed-cycle He-cryostat. For the QE measurements, light from a halogen lamp was chopped and diffracted using a 1/4 m. monochromator. A

low-noise amplifier was used both to amplify the photocurrent signal and to apply a bias voltage, V_{bias} , to the cells. V_{bias} is defined as positive when the amplifier positive terminal is connected to the p-side of the cell; i. e., we respect the sign criteria of the photo-induced voltage in a solar cell. The photocurrent detection was done using conventional lock-in techniques. For the measurement of the open-circuit voltage, V_{OC} , a He-Ne gas laser was used as a light source, providing an excitation power density of approximately one sun.

3. Results

Fig. 1b shows the measured Internal Quantum Efficiency (IQE) or External Quantum Efficiency (EQE) of the studied samples (SC1, SC2 and SC3, from left to right). Samples were measured at RT and at lower temperatures. The specific values of the temperature, T , are indicated in the figure. For each temperature, the QE was measured at different values of V_{bias} . The applied voltages, also indicated in the figure, range from 0 V to the maximum positive voltage that allowed for a tolerable noise in the measurement. Measurements are presented from 1.55 eV to lower photon energies in order to magnify the sub-bandgap part of the QE, which is more relevant in this work.

We will first briefly comment on the supra-bandgap QE. It decreases by around one order of magnitude for all samples at low temperature. We believe that the reason for the general decrease in EQE is due to non-ohmic or high-resistive behavior of the metal contacts at low temperatures. A reduction of V_{OC} must accompany the reduction in J_{SC} , however, for a particular value of T , the variation in V_{OC} for two different values of J_{SC} , J_{SC1} and J_{SC2} , is (assuming the superposition principle) equal to $\ln(J_{SC1}/J_{SC2}) \times mkT$, with $1 < m < 2$. A reduction of a factor 10 in J_{SC} would lead to a reduction of $m \times 21$ mV in V_{OC} for $T=100$ K. Therefore, the small V_{OC} variations due to the decrease in EQE can be neglected in the forthcoming discussion on voltage preservation.

All samples exhibit non-zero sub-bandgap QE at RT. The energy of the lowest-energy peak of the QE is labeled E_H , as it corresponds to the larger of the two sub-bandgaps introduced by the IB. This energy is related to transitions from the ground state (GS) for holes to the GS for electrons in the QDs. E_{ES} , in turn, corresponds to the energy of the transition between confined first excited states (ES) for holes and electrons in the QDs. This is the transition configuration found theoretically [9] and experimentally [10] for InAs/GaAs QDs; for under-terminated dot geometry the actual transitions could differ. For each

Table 1
Characteristic design features and measured and calculated parameters at $T=10$ K, unless otherwise specified, of the studied samples.

Test sample	SC1	SC2	SC3
Number of QD layers	30	10	10
Si δ -doping level (cm^{-3})	3.4×10^{15}	1.9×10^{16}	3.6×10^{16}
p-emitter doping level (cm^{-3})	2×10^{18}	2×10^{18}	2×10^{18}
n-emitter doping level (cm^{-3})	1×10^{18}	2×10^{17}	2×10^{17}
d (nm)	84	13	10
W_{QD} (nm)	2655	160	110
FDLs	No	Yes	No
FDL n doping level (cm^{-3})	–	1×10^{16}	–
E_H (eV)	1.07 ^a	1.03 ^a	1.13
E_{ES} (eV)	1.14 ^a	1.08 ^a	1.21
E_G (eV)	1.52	1.52	1.52
V_{OC} (V) at RT	0.69	< 0.47	0.68
V_{OC} (V)	1.48	1.48	1.20
F_{max} (kV/cm) at $V_{bias}=0$ V	– 34.8	– 47.5	– 146.1
F_{max} (kV/cm) at $V_{bias}=E_H/\text{eV}$, assuming $V_2=0.2/0$ V	– 14.6/– 20.0	– 4.0/– 13.7	– 60.2 ^b
F_{max} (kV/cm) at $V_{bias}=E_{ES}/\text{eV}$, assuming $V_2=0.2/0$ V	– 12.2/– 18.3	– 1.2/– 11.4	– 29.6/– 53.1

^a Extrapolated from values measured at higher temperatures.

^b The use of V_2 does not hold in this case, since the whole QD-stack lies in the SCR.

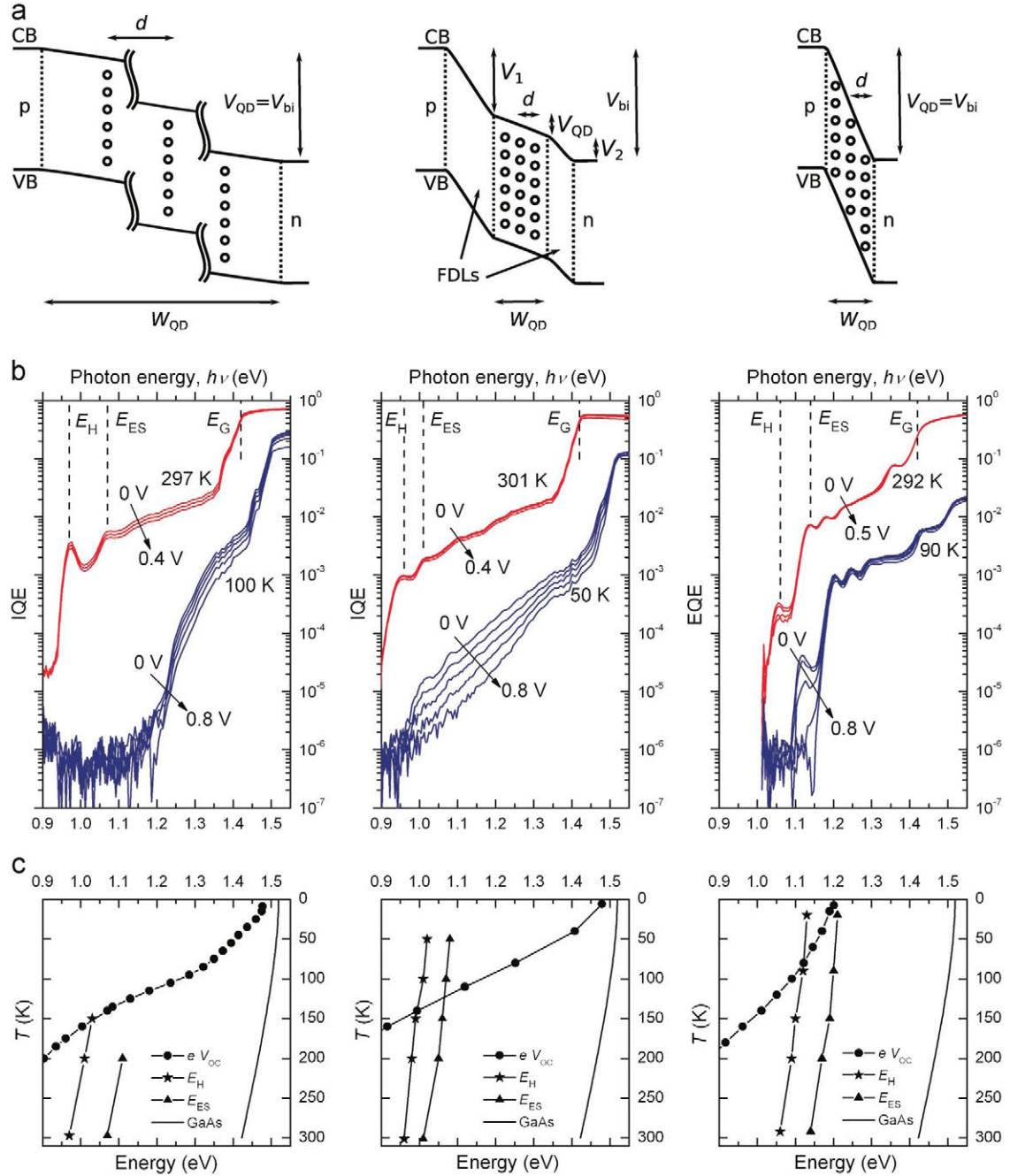


Fig. 1. From left to right: SC1, SC2 and SC3. (a) Simplified band diagram under short-circuit conditions ($V_{bias}=0$ V) of the studied samples. The thickness of the spacers between consecutive dot layers, d ; the QD-stack thickness, W_{QD} , and the potential drops in the QD-stack, V_{QD} , and in the whole structure, V_{bi} , are indicated. (b) Voltage dependency of the IQE/EQE measured at RT (red lines) and low temperature (blue lines). The range of applied voltages, V_{bias} , is indicated in each case. (c) Measured open-circuit voltage, expressed as eV_{oc} , as a function of T . The measured values of E_H and E_{ES} at different temperatures, and the theoretical value of E_G are also plotted. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

sample, E_H and E_{ES} are indicated in the QE at RT presented in Fig. 1b. The reason for the difference of these values between the samples is related to the morphology and composition of the dots, and can be found in Ref. [6]. The values for E_H and E_{ES} at 10 K are gathered in Table 1.

The application of a biasing voltage V_{bias} at RT has little or no impact on the QE of all samples. At low temperatures the QE of all samples diminishes for all photon energies; however, some important differences must be noted. The sub-bandgap QE has disappeared for SC1 (with thick barriers) at $T=100$ K. At this temperature the application of V_{bias} has a small impact on the QE, reducing it slightly. On the other hand, SC2 (with thin barriers and FDLs) still exhibits

sub-bandgap QE at 50 K and 0 V bias. However, in this case, the application of V_{bias} results in further reduction of the sub-bandgap QE. This reduction is larger for the lowest photon energies, being approximately a factor 10 for photon energies close to E_H at $V_{bias}=0.8$ V. The supra-bandgap QE of SC2, on the contrary, is not affected by V_{bias} . SC3 (with thin barriers but no FDLs) exhibits sub-bandgap QE at low temperature (90 K) as well, but the voltage dependency differs from that of SC2. In this case, the QE at the energy E_H diminishes more rapidly with V_{bias} , vanishing below the noise level at 0.8 V, which implies a reduction of at least a factor 40. For higher energies, the sub-bandgap QE remains independent of

V_{bias} . Note, in particular, that the peak at energy E_{ES} remains unchanged.

Fig. 1c presents the measured values of V_{OC} , expressed in eV, as a function of T for each sample (again SC1, SC2 and SC3, from left to right). In order to facilitate comparison with Fig. 1b, only the range 0.9–1.55 eV is represented. To help the discussion, the measured values of E_{H} and E_{ES} are also plotted. The values of the V_{OC} at RT and at 10 K are summarized in Table 1.

The V_{OC} of samples SC1 (thick spacers) and SC2 (FDLs) increase with decreasing T , exceeding E_{H}/e for T lower than 150 K. At very low temperatures both samples present a V_{OC} close to E_{C}/e and, thus, fulfill the voltage preservation principle. The V_{OC} of sample SC3 (thin spacers and no FDLs) also increases with decreasing T , and surpasses E_{H}/e at around 150 K. However, the behavior at very low temperatures is different from that of SC1 and SC2. The V_{OC} of SC3 does not approach E_{C}/e ; instead it does not surpass the value of E_{ES}/e and hence SC3 does not fulfill the voltage preservation principle.

4. Discussion

Thorough photocurrent studies of the tunnel escape of carriers in QDs embedded in a p–i–n structure can be found in the literature [11,12]. Therein, it is demonstrated that tunneling is the dominant escape process at low temperatures (thermal escape has been suppressed) and that it increases with applied reverse bias. In a triangular potential barrier the escape of carriers from a localized level within the bandgap to the CB (or the VB) has the following dependence [13]:

$$\text{tunneling rate} \propto \exp \left(- \frac{4}{3} \frac{(2m^*)^{1/2} (\Delta E)^{3/2}}{e\hbar F} \right) \quad (1)$$

where m^* is the effective mass of the carrier, ΔE is the energetic difference between the level and the edge of the closest band, \hbar is the reduced Planck's constant, and F is the existing electric field. Fig. 2 illustrates the tunnel escape of an electron from a confined level of the QD (the IB) to the CB of the barrier material. If more than one confined level exist, the tunneling rate for each of these levels will be different, since ΔE depends on the energy of the level. Thus, assuming m^* constant for all the confined levels, the tunneling rate from the IB to the CB due to F will be greater from a more energetic confined level (a level higher in the well) compared to a less energetic one. In addition, from (1), the tunneling rate has an inverse exponential dependence with F . Also from (1), the only dependence of the tunneling process with T is that coming from the dependences with m^* , ΔE and F .

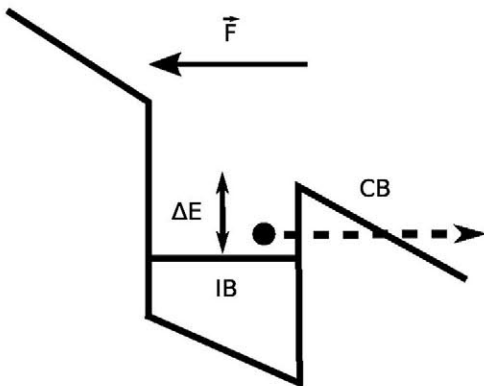


Fig. 2. Tunnel escape of an electron from a confined level of the QD (the IB) to the CB of the barrier material.

The electric field which triggers tunnel escape in IBSCs is the one originating from the potential difference, called built-in potential, V_{bi} , of the asymmetrically doped emitters. In a p–n structure, this potential difference drops in a very narrow region, called the space charge region (SCR), which expands at both sides of the junction. An internal electric field is present within the SCR. In a p–i–n structure, where the i-region is intrinsic or lightly doped, the electric field extends throughout the i-region, with only a small dependence on the doping levels of the surrounding p- and n-regions. If a QD-stack is placed in the i-region, it is subjected to the internal electric field and carrier tunneling may occur. Increasing the spacer thickness between QD-layers, d , increases the total width of the QD-region, W_{QD} . A larger W_{QD} , in turn, reduces the intensity of the electric field affecting the QD-stack, thus reducing the tunneling rate. The FDLs tested in this work aimed to sustain a substantial part of the voltage drop, thus diminishing the electric field affecting the QD-stack, without increasing W_{QD} . This phenomenon is indicated in Fig. 1a, where a distinction is made between the built-in voltage of the device, V_{bi} , and the potential drop in the QD-region, V_{QD} .

To analyze the $QE(T, V_{\text{bias}})$ and $V_{\text{OC}}(T)$ results, we have calculated, by solving Poisson's equation, the electric field present at $T = 10$ K in the studied samples as a function of V_{bias} . In our analytical model we assume: (1) a one dimensional device; (2) a step doping profile; (3) perfect ohmic contacts; (4) $V_{\text{bi}} = 1.5$ V, and (5) the full depletion approximation, which implies that the charge density is that of the ionized doping impurities in the space charge region (or regions), and zero in the semiconductor areas outside the SCR. We have performed the calculations at low temperature due to the need to compare with experimental results where thermal escape is prevented, so that the tunneling component of the carrier escape can be studied. We have chosen 10 K to illustrate the results because this is the temperature at which the measured V_{OC} is higher for all samples and determines if voltage preservation is fulfilled or not.

The application of an external voltage, V_{bias} , modifies the total potential drop in the structure (V_{bi} at short-circuit) reducing it when $V_{\text{bias}} > 0$. In the case of SC2, this reduction is distributed among V_{QD} and the potential drops in the FDLs, labeled V_1 and V_2 in Fig. 1a. In this regard, the following consideration has been taken into account in our model: the QD-stack of the studied samples is Si-doped at the concentration of one impurity per QD so that the GSs for electrons of the QDs are filled with one electron (half-filled). This means that if the QDs were in a flat-band region, the Fermi level would be located at the energy of the GS for electrons. The n-emitter is highly doped, so we can assume that the difference between the Fermi level and the CB is negligible in this region. As a consequence, the maximum potential drop between the QD-stack and the n-emitter, V_2 , is given by the energy separation between the GS for electrons and the CB; i. e., the sub-bandgap E_{L} . In our calculation we have assumed $E_{\text{L}} = 0.2$ eV, which is a reasonable value for InAs/GaAs QDs [14–16]. To obtain an enclosed range of values for the calculated electric field, we have worked with two extreme scenarios: (1) V_2 remains constant for the used values of V_{bias} , and (2) for high values of V_{bias} , V_2 is reduced to 0 V. In order to account for a positive V_2 , a charge dipole is modeled at the coordinate of the i-FDL/n-emitter interface (or QD stack/n-emitter interface, if part of the QD stack lies in a flat-band zone in the samples without FDLs, see Fig. 3 (top), for an example). We use this approximation because the width of the charged regions within the i-FDL and the n-emitter are small compared to the thickness of the whole device and we are not interested in the exact values of either the charge density, the electric field of the potential in those regions. The approximation is valid as long as the doping level of the QD region is much smaller than the doping level of the n-emitter, for reasonable values of the width of the i-FDL (in the order of 100 nm). In the samples without FDLs, if due to the applied voltage there exists a flat-band zone within the QD-stack, the

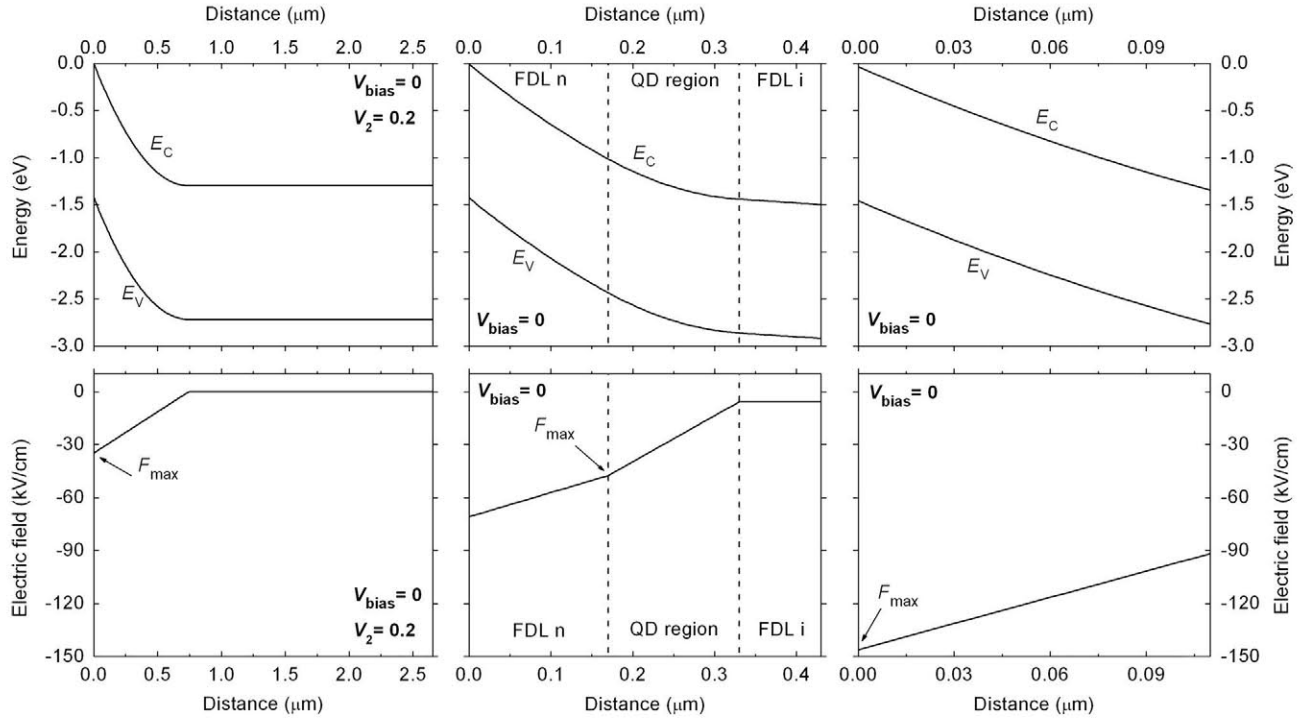


Fig. 3. Calculated band diagram (top) and electric field (bottom) of the QD region in samples SC1, SC2 and SC3 (from left to right). In the case of sample SC2 we include the FDLs. The results correspond to $V_{\text{bias}}=0$ V. E_C and E_V are the bottom edge of the CB and the top edge of the VB, respectively. The results correspond to $V_{\text{bias}}=0$ V. The peak value of the electric field in the QD region, F_{max} , is indicated.

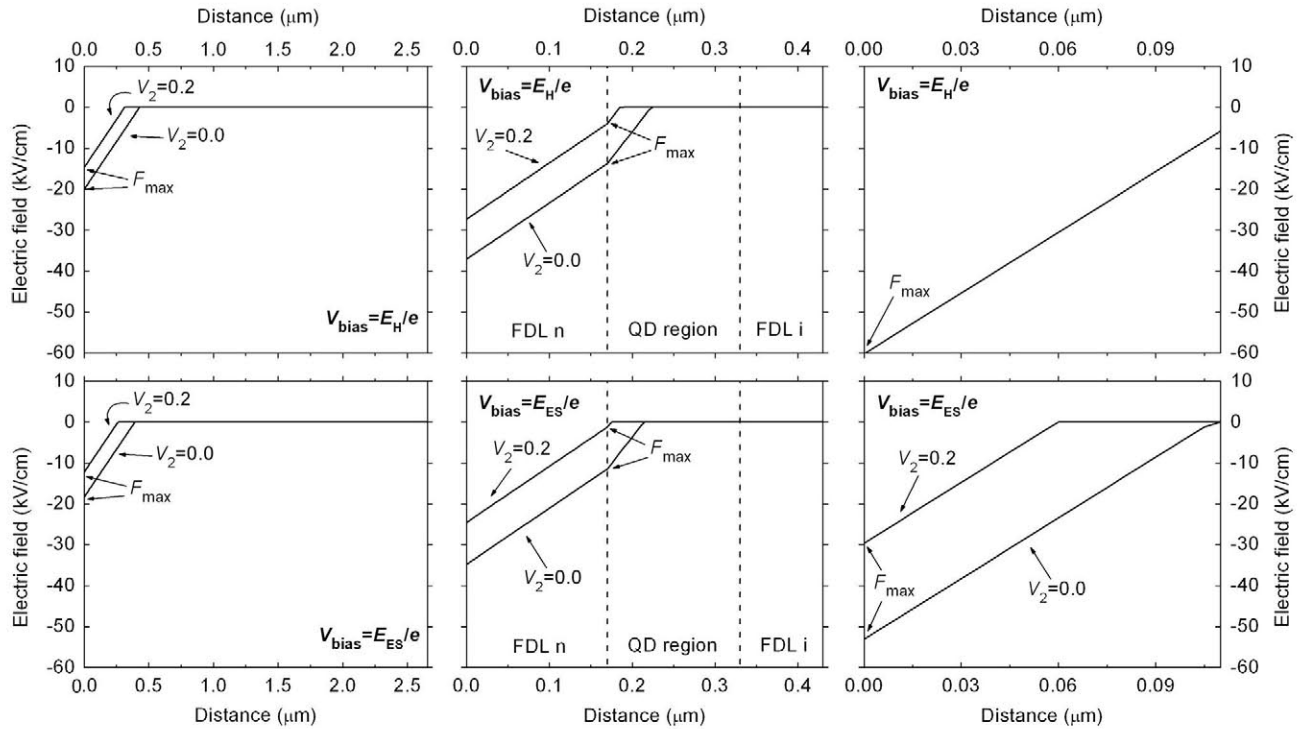


Fig. 4. Calculated electric field of the QD region (and FDLs) in samples SC1, SC2 and SC3 (from left to right) for $V_{\text{bias}}=E_H/e$ (top) and $V_{\text{bias}}=E_{ES}/e$ (bottom). In the case that a flat-band zone exists within the QD region, the two extreme cases for V_2 , 0.2 V and 0 V, are plotted. The peak value of the electric field in the QD region, F_{max} , is indicated.

possible band bending in the QD region close to the QD region/n-emitter interface is left out of our model. This is justified since the maximum potential drop in that junction is 0.2 V, much smaller than in the p-side of the device.

Fig. 3 shows the calculated band diagram (top) and electric field (bottom) of the QD region in samples SC1, SC2 and SC3 (from

left to right). In the case of sample SC2 we include the FDLs, to graphically observe their effect. These results correspond to $V_{\text{bias}}=0$ V. Note that, resulting from the large width of the QD region in sample SC1, even under short-circuit conditions, there exists a flat-band zone within the QD region. Because $V_{\text{bias}}=0$ V (equilibrium, hence the use of the Fermi level applies) only the

case $V_2=0.2$ V has been considered. For samples SC2 and SC3 the whole QD region lies within a SCR. It can be seen that the FDLs, especially the n-doped FDL, absorb a large part of the potential drop in the structure. Regarding the electric field, we can observe that its intensity decreases from left to right in the structure, i. e., going from the p-emitter to the n-emitter. As commented before, this is so because most of the built-in potential drops between the p-doped emitter and the n-doped QD-stack. Since the resulting electric field is not constant in the QD region, we will use for the discussion, its peak value, F_{\max} . This value, included in Table 1, is an upper bound that will allow us to analyze trends and compare the different results.

Fig. 4 shows anew the calculated electric field for samples SC1, SC2 and SC3 (from left to right), only this time for $V_{\text{bias}}=E_H/e$ (top) and $V_{\text{bias}}=E_{ES}/e$ (bottom). In the case that a flat-band zone exists within the QD region, the two extreme cases for V_2 , 0.2 V and 0 V, are plotted. We can observe the effect of the FDLs of sample SC2, in which already at $V_{\text{bias}}=E_H/e$ almost the intensity of F_{\max} is reduced to levels lower than for sample SC1. Conversely, for sample SC3 the electric field is still much higher than for sample SC1.

Let us now analyze our experimental results in the light of the calculated values of the electric field. At the low temperature used in the experiments thermal escape has been already inhibited [6]. From Fig. 1b, tunnel escape does not take place in SC1 either at short-circuit conditions or under positive V_{bias} , since the sub-bandgap QE has vanished. F_{\max} is -34.8 kV/cm for $V_{\text{bias}}=0$ and is not large enough to produce measurable tunnel escape. For SC2, F_{\max} is -47.5 kV/cm at short-circuit conditions. This value is higher than the one obtained for SC1, but not as high as it could be expected taking into account the large difference in W_{QD} . It indicates that the FDLs are effective, sustaining part of V_{bi} and reducing the electric field in the QD region. As deduced from the QE results, the electric field is high enough to allow some carrier tunneling in SC2 since, although small, sub-bandgap photocurrent is detected. With positive V_{bias} , the intensity of F_{\max} diminishes more rapidly than for the case of SC1 (see Table 1 and Fig. 4), again due to the presence of the FDLs. As a consequence, tunnel escape (and so the QE) is strongly reduced. Note that for $V_{\text{bias}}=E_H/e$ (1.03 V) and $V_{\text{bias}}=E_{ES}/e$ (1.08 V), F_{\max} has been reduced to $-4/-13.7$ kV/cm and $-1.2/-11.4$ kV/cm, respectively. The QE measurements show that at $V_{\text{bias}}=0.8$ V, tunnel escape is no longer measureable for the lowest sub-bandgap energies.

The value of F_{\max} at short-circuit is -146.1 kV/cm for SC3. It is much higher than those obtained for SC1 and SC2 because of the small W_{QD} and the absence of FDLs in this sample. Consequently, fast tunnel escape is allowed, as can be deduced from the QE results, where a relatively high sub-bandgap QE is shown even at 90 K. F_{\max} is reduced with positive V_{bias} but it remains much higher than for the other two samples. The calculated values are -60.2 kV/cm and $-29.6/-53.1$ kV/cm for $V_{\text{bias}}=E_H/e$ (1.13 V) and $V_{\text{bias}}=E_{ES}/e$ (1.21 V), respectively. In the QE measurements we can see that tunnel escape

has been inhibited for photons with energy E_H at $V_{\text{bias}}=0.8$ V, which means that, at this voltage bias, the electric field is *not* large enough to produce tunnel from the GS to the CB. Conversely, the sub-bandgap QE for photons with energy E_{ES} (or higher) is not affected. This means that for the V_{bias} , the electric field is high enough to produce a fast tunnel escape between the ES and the CB. As explained before, this is due to the negative exponential dependency of the tunnel escape with ΔE .

Sample SC2 presents tunnel carrier escape at short-circuit conditions and it also achieves a V_{OC} close to E_G/e at low temperatures. The explanation is as follows. Provided that thermal escape is inhibited, the key factor to preserve the voltage is that, in general, tunnel escape from a QD confined state, ϵ_{CS} , must be inhibited when the photo-induced voltage is close to the energy gap between the VB and ϵ_{CS} (labeled E_{QD} in Fig. 5). If tunnel escape from ϵ_{CS} to the CB still occurs under photo-induced voltages close to E_{QD}/e , the IB and the CB are electrically connected and a quasi-Fermi level split between those two bands is not possible (Fig. 5a). In this case the QDs fundamentally limit the maximum V_{OC} attainable by the IBSC, $V_{\text{OC,max}}$, to E_{QD}/e . If V_{OC} exceeds E_{QD}/e , population inversion would be achieved in the IB, leading to stimulated emission. On the other hand, if tunnel escape is sufficiently reduced under positive voltage so that two distinct quasi-Fermi levels, ϵ_{Fe} and ϵ_{FIB} , are needed to describe the electronic populations of the CB and the IB, respectively, (Fig. 5b) the photo-voltage can exceed E_{QD}/e since at least the excess of voltage ($V_{\text{OC}}-E_{\text{QD}}/e$) would be used in splitting them; this is, $\epsilon_{\text{Fe}}-\epsilon_{\text{FIB}} \geq eV_{\text{OC}}-E_{\text{QD}}$. In this case, the IB created by the QDs does not impose a fundamental limitation to $V_{\text{OC,max}}$, which remains equal to E_G/e . Indeed for those quasi-Fermi levels to decouple, not only thermal excitation but also thermal relaxation must be inhibited. In QD physics the latter phenomenon is called *phonon bottleneck effect* [17] and consists of a reduction in the efficiency of electron de-excitation via the emission of phonons, due to the zero density of states between confined states in the potential well. A study of the impact of the phonon bottleneck effect in QD-IBSCs can be found in Ref. [18].

Sample SC3 is a good example supporting the discussed theory. It presents tunnel at short-circuit conditions for all photon energies between E_H and E_G . With positive V_{bias} tunnel escape for energies between E_H and E_{ES} is inhibited, but it remains for energies higher than E_{ES} . Not surprisingly, the V_{OC} of this sample can exceed E_H/e but not E_{ES}/e . At photo-induced voltages close to E_H/e there is no obstacle for the V_{OC} to continue increasing. However, at photo-induced voltages close to E_{ES}/e , tunnel escape from the ES to the CB is still possible and, therefore, V_{OC} cannot surpass this value.

We can now understand the relationship between the sub-bandgap QE, carrier escape and V_{OC} . If the QE at RT shows sub-bandgap QE efficiency that disappears at low temperature, it indicates the existence of thermal escape at RT. For a temperature at which thermal escape is not the dominant escape mechanism, voltage-biased QE measurements may be necessary to discard the IBSC under test as capable of achieving voltage preservation. If under

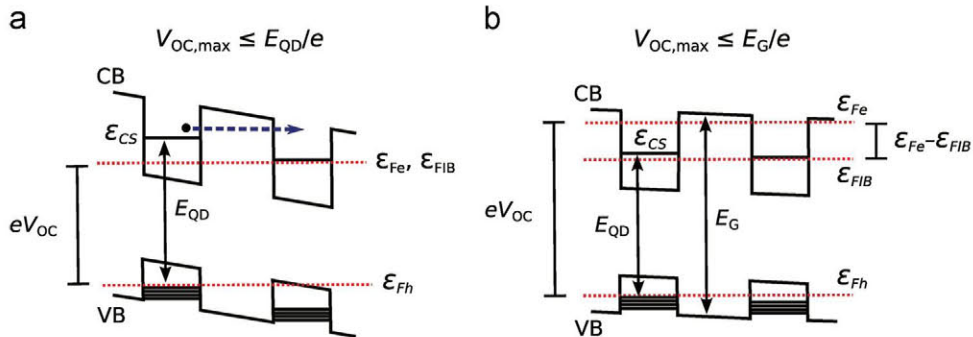


Fig. 5. Simplified band diagram of the QD-stack of a QD-IBSC under operation for the case: (a) where tunnel escape takes place under a photo-induced voltage E_{QD}/e , setting an upper limit to V_{OC} equal to E_{QD}/e and (b) where tunnel escape has been inhibited due to a photo-induced voltage E_{QD}/e , allowing V_{OC} to reach values close to E_G/e .

positive V_{bias} the tunnel-assisted sub-bandgap QE disappears, there is no carrier-escape-related limitation to the V_{OC} of the IBSC.

5. Conclusions

FDLs have been demonstrated as a useful approach for preventing tunnel carrier escape in IBSCs, which is essential for fulfilling the voltage preservation principle. In this respect, the FDLs allow the growth of QD-stacks with thin spacers, which, from a technological point of view, is convenient if a large number of QD layers need to be stacked in order to increase sub-bandgap absorption. The dependence of the QE with an external applied voltage has been studied and the electric field affecting the QD-stack of the studied samples has been calculated.

The use of FDL reduces the potential drop in the QD-stack and the associated electric field. Our calculations, at low temperature, show that the maximum intensity of the electric field under short-circuit conditions is 47.5 kV/cm for the sample with thin spacers and FDLs and 146.1 kV/cm for the sample with thin spacers and no FDLs, to be compared with 34.8 kV/cm for the sample with thick spacers. Under applied voltages of E_{it}/e and E_{es}/e , the maximum intensity of the electric field is reduced to 4.0–13.7 kV/cm and 1.2–11.4 kV/cm, respectively, for the sample with FDLs, and to 60.2 kV/cm and 29.6–53.1 kV/cm, respectively, for the sample without FDLs. The strong reduction in the electric field totally suppresses tunnel carrier escape in the sample with FDLs, enabling voltage preservation. However, tunnel carrier escape from confined states is still present in the sample without FDLs under the applied voltages, which explains the limitation to the output voltage in the V_{OC} measurements and why this sample does not fulfill the voltage preservation principle.

From the results obtained, a theory describing the evolution of the QE with the possibility of voltage preservation has been developed. The conclusion is that tunnel carrier escape will only limit the output-voltage to values close to E_{it}/e if it still takes place when the photo-voltage of the IBSC reaches this value. It has been demonstrated that the presence of tunnel carrier escape under short-circuit conditions is not definite proof of the impossibility of an IBSC of fulfilling voltage preservation.

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